25.1 A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing

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State-of-the-art mobile communication systems need power-efficient ADCs. Both low power consumption and minimum supply voltage are very important since mobile systems are battery operated. Technology scaling can support increased bandwidth requirements, but the corresponding reduction in supply voltage makes analog design critical [1]. One of the most critical parts is the amplifier, so a comparator-based switched-capacitor circuit [2] or a digitally corrected analog design [3] are published as alternatives in nm technologies to allow low supply voltage operation. However, fundamental analog design techniques are still important because primary performance is restricted by the analog part. This paper describes a low supply voltage design that was developed for amplifiers in a pipelined ADC, regulating overdrive voltage (V_{od}; V_{od} is given as $V_{od}=V_{gs}-V_{th}$) to be constant against PVT conditions. The ADC operates at 10b 80MS/s from a 0.8V supply without digital calibration.

Generally, the dynamic range of the signal in analog circuits such as amplifiers reduces with supply voltage. However, the thermal noise, represented by kT/C, stays constant. Therefore, in order to get the same SNR, a lower thermal noise level is needed. But this increases supply current, because a larger capacitance and/or higher g_m is needed. As a result, lower supply voltage does not always result in lower power consumption. Analog circuit design that improves dynamic range is important for low supply voltage systems.

Signal dynamic range is set by the supply voltage minus the V_{od} of transistors in the current path. So, reducing the number of cascaded transistors in the current path increases signal dynamic range. However, it restricts analog circuit topology, for example cascaded topology that is used to improve performance. High V_{od} degrades dynamic range and low V_{od} may increase noise and/or mismatch. V_{od} is influenced by PVT when current is constant. If V_{od} is regulated constant against PVT, multiple cascaded topologies can be applied, fixing these dynamic range, noise, and mismatch problems.

The relationship between V_{od}, β and current Id is given as, $Id = (\beta/2) * V_{od}^2$. β is influenced by temperature and process condition, however, if current is controlled to compensate for this, V_{od} can remain constant. Figure 25.1.1 shows the principles of regulated overdrive voltage biasing (ROB). The channel width of M2 is 4× larger than that of M1. The negative feedback loop regulates V_{od} of M1 and M2 to force I1 and I2 to be identical, because the current is mirrored by M3 and M4. This means that any V_{od} can be set to equal Vn. In this design Vn=90mV is used. The output Vb3 is used to bias NMOS current sources via common-mode feedback (CMFB) circuits to keep the V_{od} constant. Although bandwidth and power consumption vary over β by using ROB, regulating V_{od} constant allows low supply voltage operation.

Figure 25.1.2 shows the schematic of a 2-stage amplifier, which is implemented in the MDAC part of the pipelined ADC. The first stage generates large DC gain, restricting the signal swing. The second stage provides large dynamic range. Cascaded topology is indispensable for higher gain of the first stage. The ROB technique enables implementation of a cascaded topology in the first stage, which is free from PVT issues.

A folded-cascode and gain-boosting technique are applied in the first stage of the amplifier for higher gain. The input pair, M5 and M6, is implemented using PMOS transistors, to increase second-pole frequency and reduce 1/f noise. This schematic has 4 cascaded transistors, but they are controlled by the ROB technique so that they remain in saturation over PVT. Push-pull topology with single PMOS and NMOS is used on the second stage for larger dynamic range. This provides common-mode control, and the g_m can be approximately twice that of a single-ended common-source topology.

The input common mode level of the second stage needs to tolerate the distribution of the first stage output-common mode level caused by process variation. If the first and second stages are connected directly, the output common-mode level of the first stage will vary by several hundred-mV with threshold-voltage variation. However, this is hard to design over PVT at a low supply voltage, so 2 switched-capacitor level-shift circuits [4] are connected between the first stage and the second push-pull stage. This enables the output common-mode level of the first stage to be independent of the second-stage input common-mode level. Cascode compensation is used with the g_m of the first stage PMOS cascodes providing pole-zero cancellation. This design achieves $1.2V_{pp}$ differential output level with 76.8dB of DC gain at 0.8V supply in simulation.

Figure 25.1.3 shows the ADC architecture. It has 7 stages of 1.5b per stage with digital correction and a final 3b flash ADC. The sample-and-hold block and MDAC are fully differential and use double sampling. The switched-capacitor level-shift circuits in figure 25.1.2 are designed for interleaved operation, required by the double-sampling architecture. The prototype ADC is fabricated in 1P10M 90nm CMOS with MIM capacitors. A micrograph of the chip is shown in Fig. 25.1.4. The active area is $1.18\times0.54mm^2$.

Figure 25.1.5 shows the SNDR as a function of supply voltage with analog input frequency of 21MHz and a conversion rate of 80MS/s. SNDR remains above 53dB down to 0.76V supply voltage. Figure 25.1.6 (a) shows the SNDR as a function of analog input frequency with 0.8 to 1.2V supply voltage at 80MS/s. The peak SNDR at 0.8V supply is 55.0dB at 2MHz analog input frequency and 51.4dB at 41MHz input frequency. SNDR decrease with input frequency is <3.6dB up to the Nyquist frequency. Figure 25.1.6 (b) shows the SNDR as a function of conversion rate at 0.8V supply with analog input frequencies of 11MHz and 41MHz. SNDR degradation remains below 3.0dB up to 110MS/s. Power consumption at 80MS/s and 41MHz input frequency is 6.5mW with 0.8V and 13.3mW with 1.2V supply, respectively. Figure 25.1.7 summarizes the performance.

References:

[1] K. Bult, "Analog Design in Deep Sub-Micron CMOS," *Proc. ESSCIRC*, pp. 126-132, Sep., 2000.

[2] T. Sepke, J.K. Fiorenza, C.G. Sodini, et al., "Comparator-Based Switched–Capacitor Circuits for Scaled CMOS Technologies, " *ISSCC Dig. Tech. Papers*, pp. 220-221, Feb., 2006.

[3] B. Murmann, B. Boser, "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2040-2050, Dec., 2003.

[4] R. Castello, P. R. Gray, "A High-Performance Micropower Switched-Capacitor Filter," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1122–1132, Dec., 1985.

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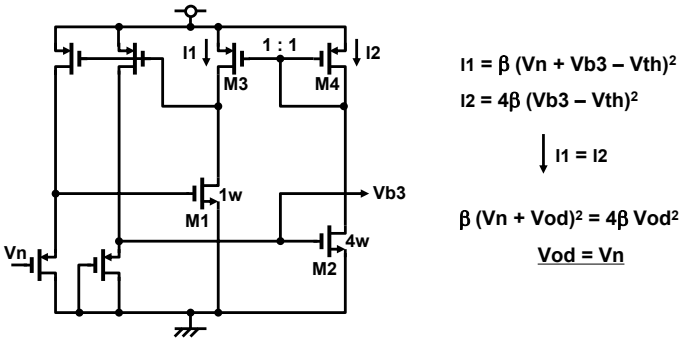


Figure 25.1.1: Principle of regulated overdrive voltage biasing (ROB).

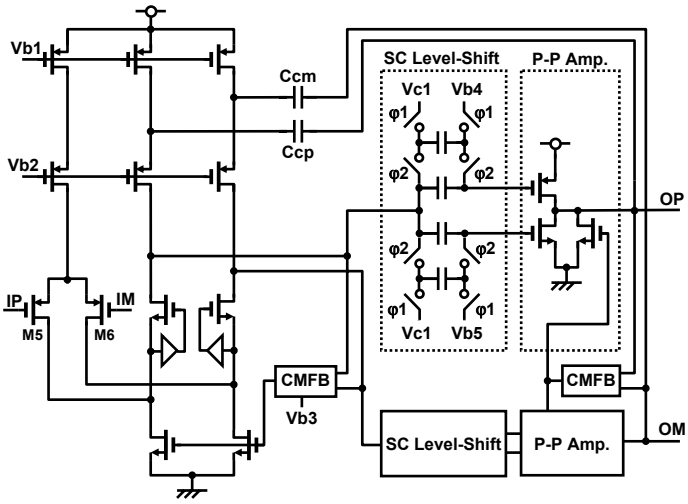


Figure 25.1.2: Schematic of two-stage amplifier.

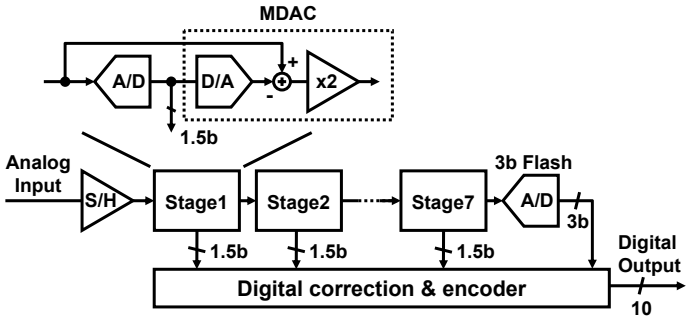


Figure 25.1.3: ADC block diagram.

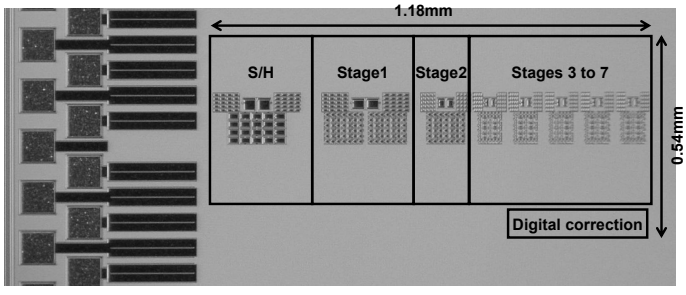


Figure 25.1.4: Chip micrograph.

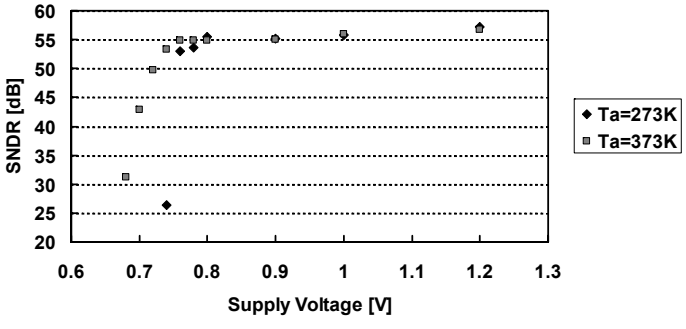


Figure 25.1.5: SNDR versus supply voltage at 80MS/s with 21MHz Input.

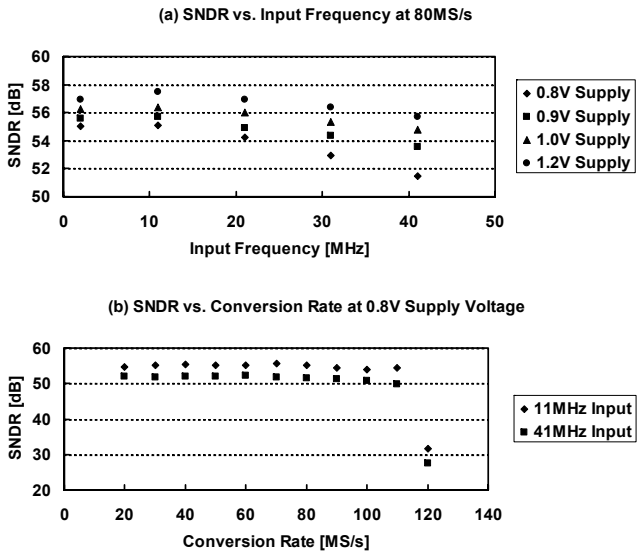


Figure 25.1.6: SNDR versus input frequency or conversion rate.

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Technology	1P10M 90nm CMOS with MIM capacitors	
Resolution	10b	
Conversion Rate	80MS/s	
Active Area	1.18 x 0.54mm^2	
Input Range	1.2V$_{pp}$ Differential	
Supply Voltage	0.8V	1.2V
SNDR	55.0dB @ 2MHz Input 51.4dB @ 41MHz Input	56.9dB @ 2MHz Input 55.6dB @ 41MHz Input
Total Power Consumption	6.5mW	13.3mW
INL	< 1.0LSB	< 0.5LSB
DNL	< 0.8LSB	< 0.4LSB

Figure 25.1.7: Summary of ADC performance.

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